CURRENTLY PENDING CLAIMS

1. (Previously Amended) A system comprising:

a memory bus; and

a plurality of memory controllers, each memory controller to generate memory requests on the memory bus according to a predetermined priority scheme,

at least two of the plurality of memory controllers adapted to generate concurrently pending memory requests on the memory bus.

2. (Original) The system of claim 1, wherein the predetermined priority scheme comprises a time slot priority scheme.

3. (Original) The system of claim 1, wherein the predetermined priority scheme comprises a request-select priority scheme.

4. (Original) The system of claim 1, wherein the memory bus comprises a Rambus channel.

5. (Original) The system of claim 1, wherein each memory controller generates a memory request during a different predetermined time slot.

6. (Original) The system of claim 1, wherein the memory bus comprises plural control portions, each of the control portions associated with corresponding time slot priority schemes.

7. (Original) The system of claim 6, wherein the time slot priority schemes are staggered.

8. (Original) The system of claim 6, wherein the control portion comprise a row portion and a column portion.

9. (Original) The system of claim 1, wherein the memory bus comprises plural portions, each portion associated with a set of memory devices.

10. (Original) A system comprising:

a memory bus; and

a plurality of memory controllers connected to the memory bus, each memory controller to monitor memory requests generated by another memory controller in performing memory-related actions.

11. (Original) The system of claim 10, wherein the memory-related actions comprise a read-modify-write transaction.

12. (Original) The system of claim 10, wherein the memory-related actions comprise a cache coherency action.

13. (Original) The system of claim 10, wherein the memory-related actions comprise a memory request.

14. (Original) The system of claim 10, the memory controller to determine if the memory bus is available based on outstanding requests from other memory controllers.

15. (Original) A method comprising:

providing multiple memory controllers on a memory bus;

generating requests, by the memory controllers, on the memory bus; and

each memory controller monitoring memory-related actions by at least another memory controller.

16. (Original) The method of claim 15, wherein generating the requests comprises generating Rambus command packets.

17. (Original) The method of claim 15, wherein generating the requests comprises the memory controllers generating the requests one at a time according to a predetermined priority scheme.

18. (Original) The method of claim 17, wherein generating the requests comprises generating the requests according to a time slot priority scheme.

19. (Original) The method of claim 17, wherein generating the requests comprises generating the requests according to a request-select priority scheme.

20. (Previously Amended) The method of claim 15, further comprising each memory controller determining when to generate a memory request based on the monitoring.

21. (Previously Amended) The method of claim 15, further comprising each memory controller determining if a lock has been asserted due to presence of a read-modify-write transaction.

22. (Previously Amended) The method of claim 15, further comprising each memory controller performing a cache coherency action based on the monitoring.

23. (Original) An article comprising one or more storage media containing instructions that when executed cause a memory controller to:

monitor memory requests from another memory controller on a memory bus;

determining if a memory request can be generated on the memory bus based on the monitoring.

24. (Previously Added) The system of claim 1, wherein the plurality of memory controllers are connected to the memory bus.

25. (Previously Added) The system of claim 1, wherein one of the at least two memory controllers is adapted to generate its memory request on the memory bus before data is returned for the memory request of the other one of the at least two memory controllers.

26. (Previously Added) The system of claim 10, wherein at least two of the memory controllers are adapted to generate concurrently pending memory requests on the memory bus.

27. (Previously Added) The system of claim 26, wherein one of the at least two memory controllers is adapted to generate its memory request on the memory bus before data is returned for the memory request of the other one of the at least two memory controllers.

28. (Previously Added) The method of claim 15, wherein generating the requests on the memory bus comprises at least two of the memory controllers generating concurrently pending requests on the memory bus.

29. (Previously Added) The method of claim 28, wherein generating concurrently pending requests comprises one of the at least two memory controllers generating its request before data is returned for the request of the other of the at least two memory controllers.

30. (Previously Added) The article of claim 23, wherein the memory controllers are connected to the memory bus.